GX85RS128 SPI Interface Ferroelectric Randomized Memory (FRAM)

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1 Product Description

The FRAM chip (Ferroelectric Random Access Memory)is configured as a 16,384 × 8-bit, non-volatile memory cell formed by the ferroelectric process and the silicon gate CMOS process technology. Unlike SRAM, the chip does not require a battery to hold data.

The memory cell used in this chip can be used for 1E6 read/write operations*1. Its read/write endurance greatly exceeds that of FLASH and EEPROM, and it does not require a long time to write data like FLASH or EEPROM, and it does not require a wait time.

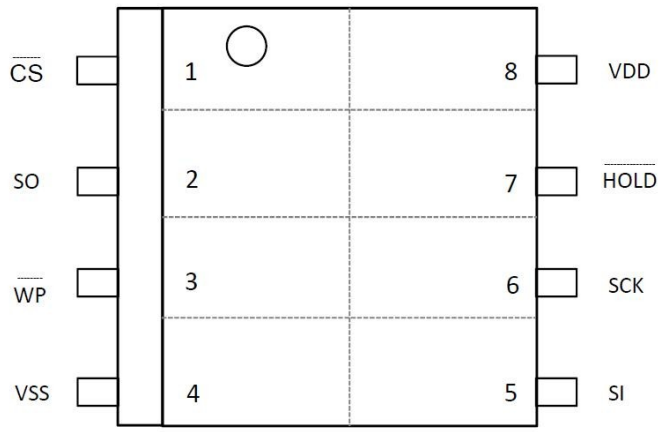
2 Product Features

quantitative (science)	128Kb
Interface Type	SPI interface (mode 0 and mode 3)
operating voltage	2.7 volts to 3.6 volts
operating frequency	25 MHz
power wastage	4.2 mA (25 MHz)
low power	9 microamps (standby)
durability	10^6 read/write (ambient), 109/read (ambient)
Data retention	10 years @ 85°C (200 years @ 25°C)
High-speed read characteristics	Supports 40MHz high-speed read commands
Operating temperature range	-40°C to 85°C
Package form	8-pin SOP package, RoHS compliant

Instructions for use:

Since FRAM storage operates with a destructive readout mechanism, the minimum value of endurance is defined here as the sum of the number of reads and writes.
We recommend programming within the temperature range. Extended operation beyond the temperature range will not guarantee data written within normal temperatures.
Data prior to reflow is not guaranteed and is only supported for one reflow. See the General Specification for Reliability Testing Techniques for more detailed instructions on use.

3 Pinouts



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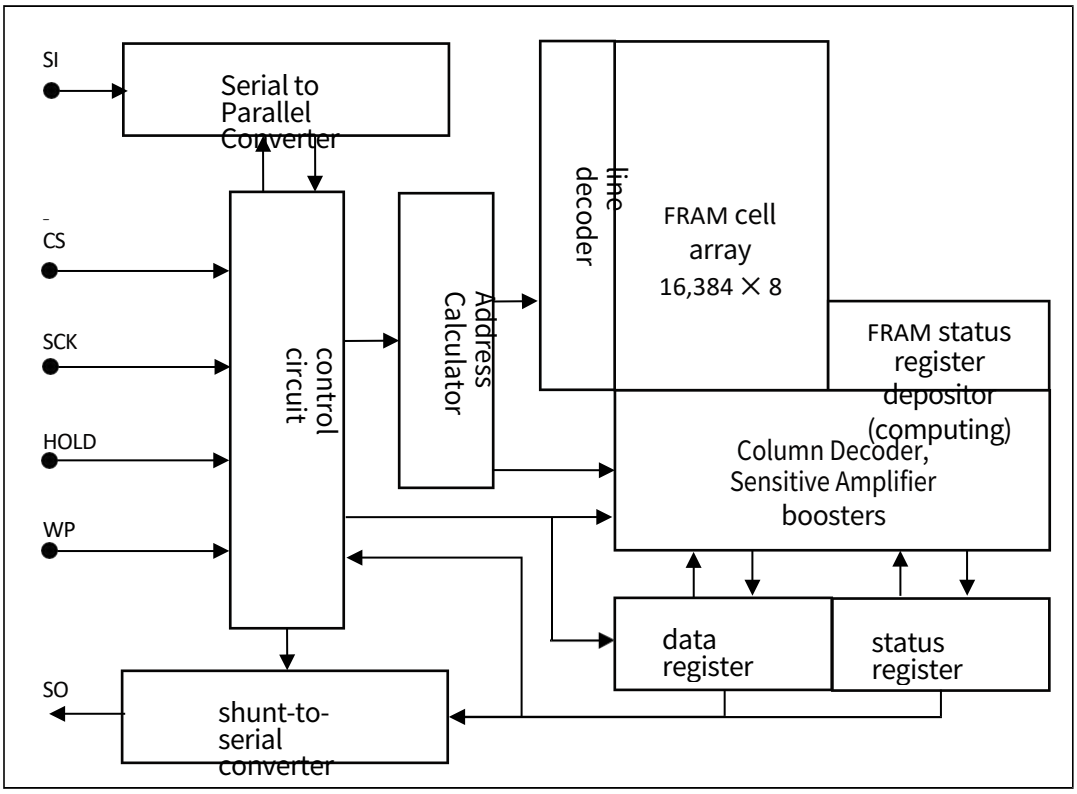
4 Pin Function Description

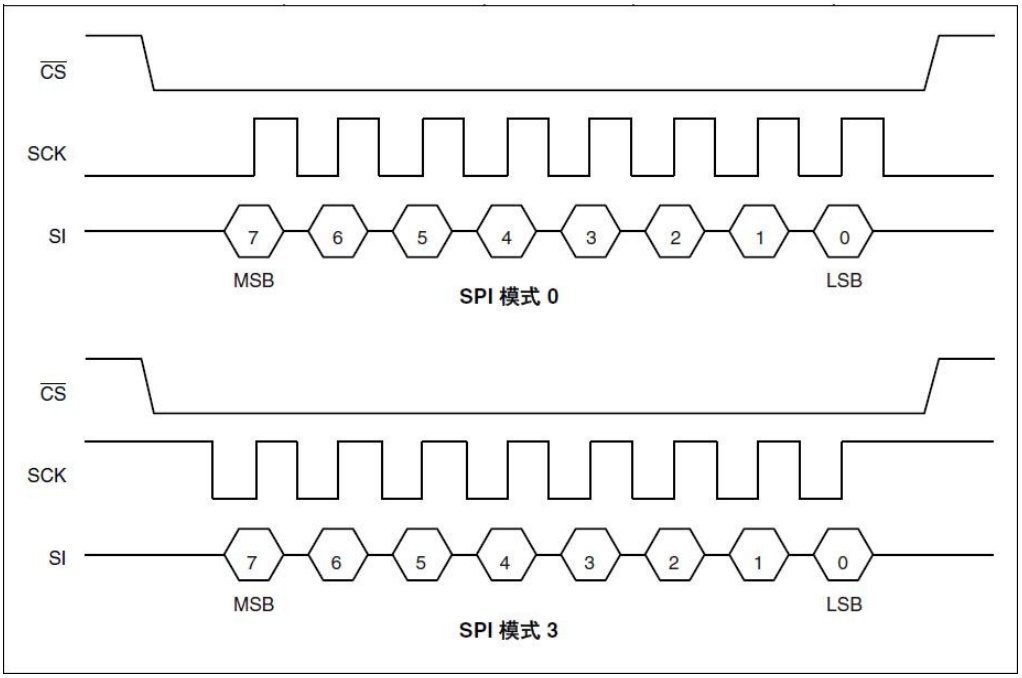
Pin Name	Functional Description
CS	chip select pin This is the input pin for chip select. When CS is at the "high" level, the device is deselected (etc.). The SO becomes a high impedance state. At this time, the chip ignores the data input from other pins. CS is The device is in the select (active) state at the "low" level. CS must be "low" before an opcode can be entered. Level. The chip select pin is internally pulled up to the VDD pin.
SO	Serial Data Output Pin
WP	Write-protect pin
VSS	ground pin
SI	Serial Data Input Pins This is the input pin for serial data. It is used to input opcode, address and data.
SCK	Serial Clock Pins Clock input pin that provides clock signals for serial data input and output.
HOLD	Hold pin, interrupts the serial input/output without canceling the chip select; when HOLD is low, the serial input/output is interrupted. The hold operation is activated, SO becomes high impedance, and SCK and SI become negligible. During the hold operation, SO becomes high impedance and SCK and SI become negligible. CS must be held low when the
VDD	Supply Voltage Pin

5 Product Block Diagram



6 interface mode

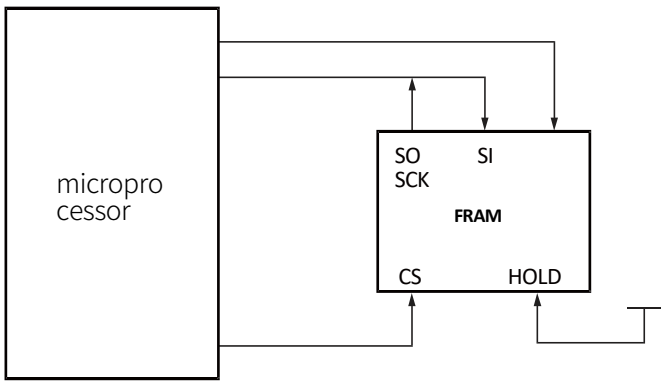
The chip supports SPI mode 0 (CPOL=0, CPHA=0) and SPI mode 3 (CPOL=1, CPHA=1)



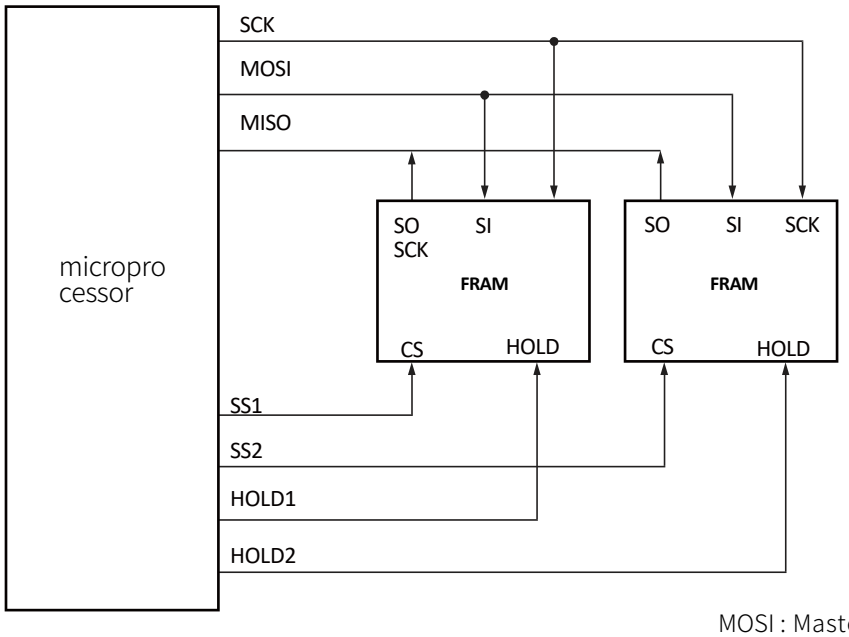
communication.

7. Serial Peripheral Interface

The chip acts as an SPI slave. Multiple devices can be connected by using a microcontroller equipped with an SPI port. Using a microcontroller that is not equipped with an Microcontrollers with SPI ports can be operated by emulating the SPI bus.



System Configuration
without SPI Interface



MOSI : Master
Output Slave Input
MISO : Master Input
Slave Output
SS : Chip Select

System **Configuration**
Using the SPI Interface

8 opcode

The chip accepts **7** types of commands specified in the opcode. The opcode is an 8-digit code, so do not enter any invalid code other than these.

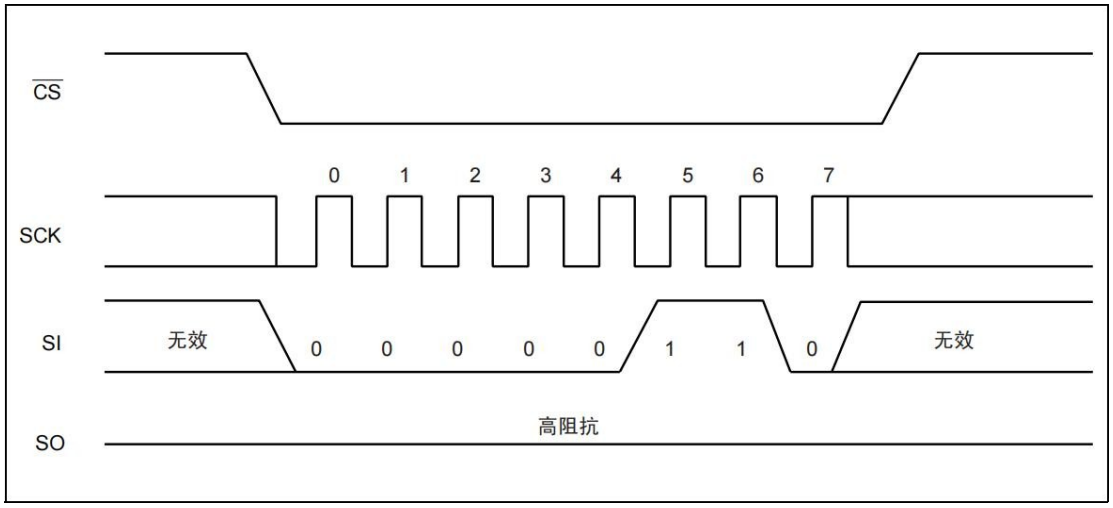
Code. If CS rises while an opcode is being entered, the command will not be executed.

command name	Command Description	opcode
WREN	Write Enable Latch Command	0000 $_{0110B}$
WRDI	Reset Enable Latch Command	0000 $_{0100B}$
READ	read command	0000 $_{0011B}$
WRITE	write an order	0000 $_{0010B}$
RDID	Read Device Serial Number Command	1001 $_{1111B}$
FSTRD	High-speed read command	0000 $_{1011B}$
SLEEP	Sleep command	1011 $_{1001B}$

9 command list

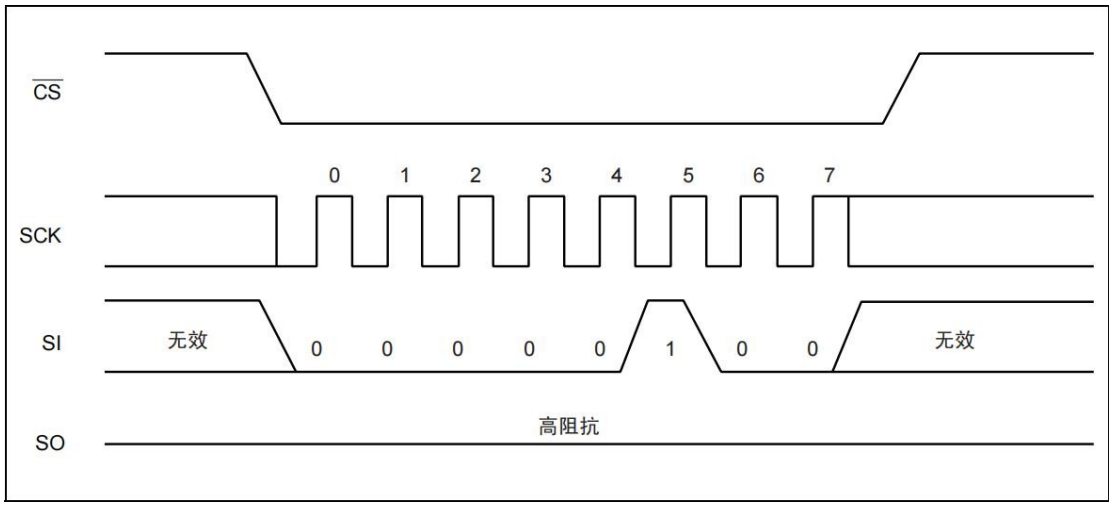
WREN

The WREN command is used to set the write enable latch. The WREN command is required to set the write enable latch before a write operation (WRITE command).



WRDI

The WRDI command is used to reset the write enable latch. No write operation is performed while the write enable latch is reset (WRITE command).

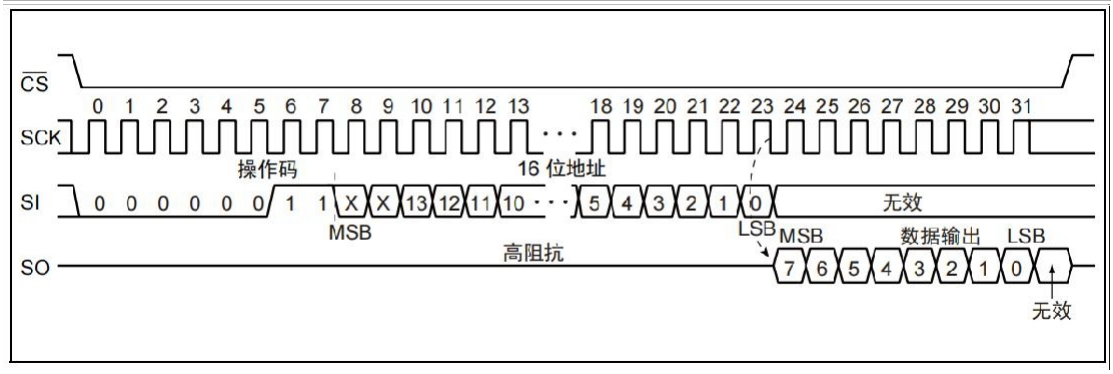


READ

The READ command reads the FRAM memory cell array data. Any 16-bit address and READ opcode are input to SI. 2 high address bits are invalid. Then, input SCK for 8 clock cycles and output SO synchronously on the falling edge of SCK.

Effective. When CS goes up, the READ command completes, but continues to read in an automatic address incremental fashion (by starting the command with

(8 cycles in units of continuous clock sending to SCK is implemented). Flips to the start address when the highest bit address is reached and holds the read cycle indefinitely.

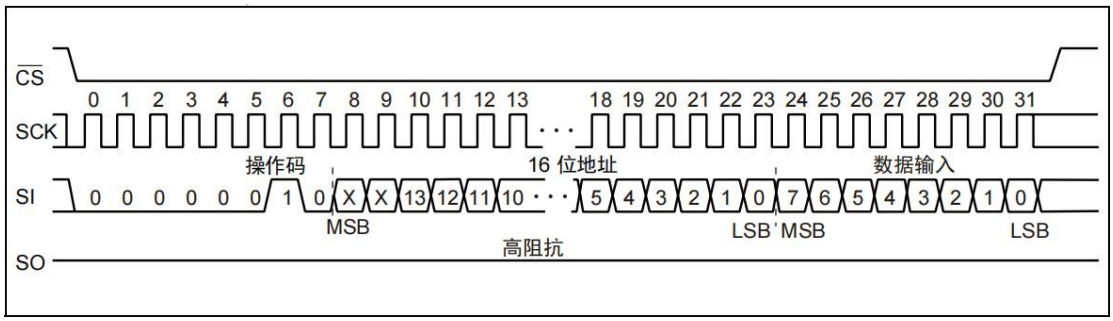


WRITE

The WRITE command writes data to the FRAM memory cell array.The WRITE opcode, any 16-bit address, and 8 bits of write data are entered into the SI, with the 2-bit high address bit invalid.

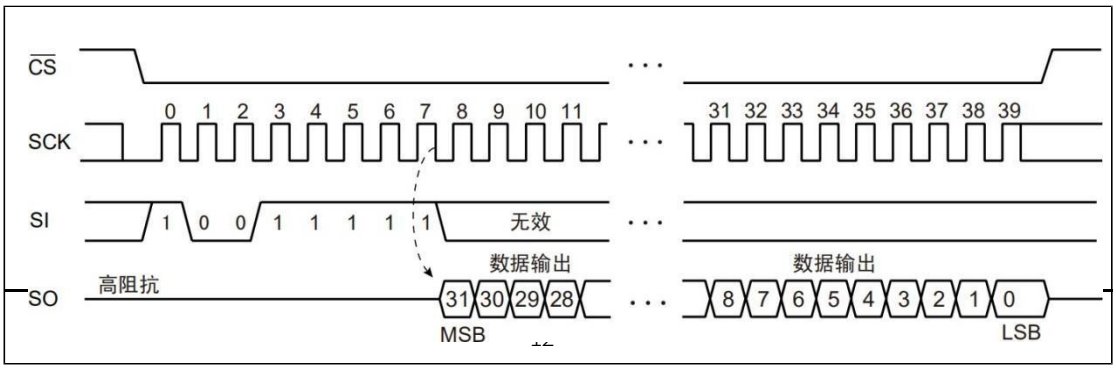
When 8-bit write data is entered, the data is written to the FRAM memory cell array. cs up will terminate the WRITE command, but the WRITE command will be terminated if

Continuing to send 8-bit write data before each CS goes up allows you to continue writing using the auto-incrementing address. When the most significant address when flipped to the start address, the write cycle will continue endlessly.



RDID

The RDID command reads the device serial number. After the RDIO command is sent to the chip，32 clocks are then sent, at which point the SI is invalidated. Data is output synchronously from the SO interface starting on the falling edge of the 8th clock. Chip ID: hex 628C 2200



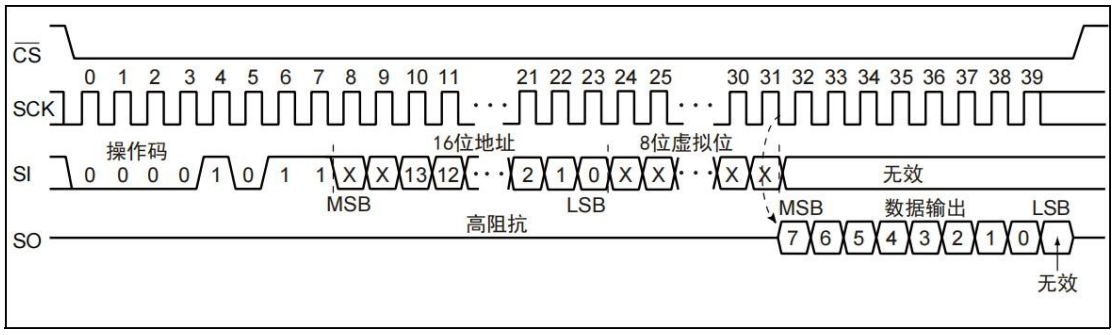
FSTRD

The FSTRD command reads data from the memory array continuously. After the 8-bit opcode, the 16-bit address information is input via the SI pin (the upper 2 bits of which are invalid), and then the 8-bit invalid data is input. At the same time as the 8-bit invalid data is input, an 8-bit clock is input to the SCK pin.

Input. On the falling edge of 8-bit SCK, the SO pin starts to output data. The SI pin is invalidated while the read is acquired. When the CS pin

pin is pulled up and the FSTRD command is terminated. Until the CS pin is pulled up, the data will be read continuously, the address will be incremented automatically, and the memory will be read cyclically.

data from the storage array.



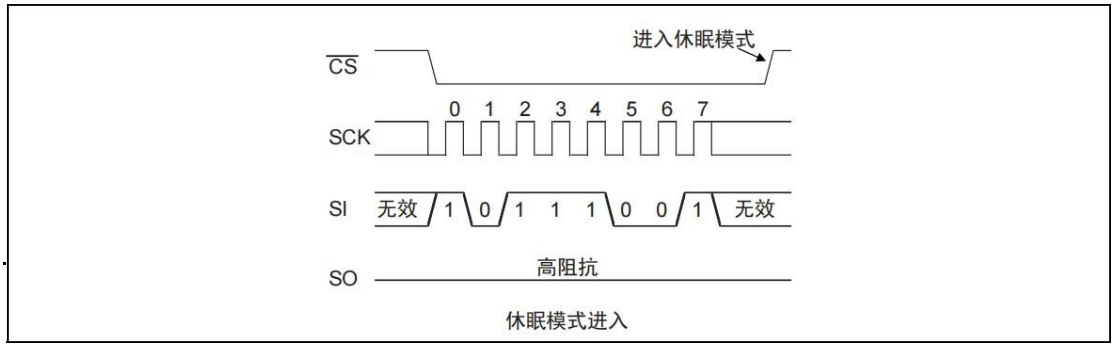
SLEEP

The SLEEP command sets the chip to sleep mode. After the opcode of the SLEEP command is executed, the rising edge of CS, the chip

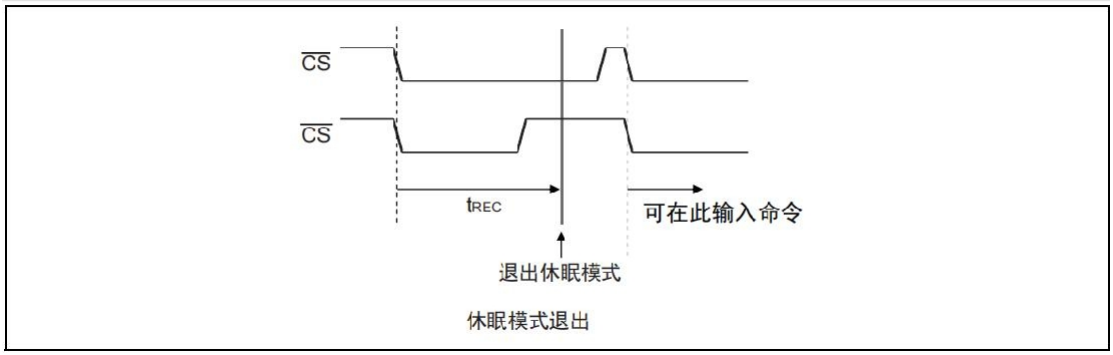
Enter sleep mode. However, after the opcode, before pulling the CS pin high, as long as there is one clock cycle of clock inputs

The SLEEP command will be canceled if you enter the SLEEP command.

Once switched to sleep mode, the inputs to the SCK pin and SI pin become invalid and SO is High-Z.



The chip exits sleep mode during the t_{REC} (maximum 1 microsecond) after the falling edge of CS.



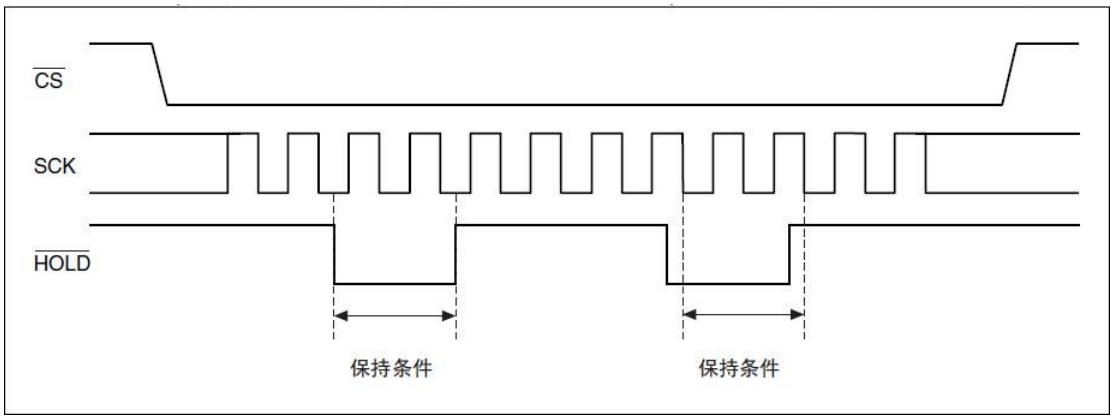
10 Holding operation

Translates the HOLD pin low to enter the hold state while SCK is low; then, while SCK is low

Returning the HOLD pin to a high level exits the hold state. Entry\exit from the hold mode is prohibited while SCK is high.

Arbitrary command operations are interrupted in the hold state, and SCK and SI inputs become ignored. SO becomes high impedance on read commands (RDSR, READ).

In addition, pulling up the CS pin during the hold state is prohibited.



11 Absolute maximum rating

parameters	notation	rating		unit (of measure)
		minimum value	maximum values	
Power supply voltage*1	V_{DD}	-0.5	4.0	V
Input Voltage*1	V_{IN}	-0.5	V_{DD} + 0.5	V
Output Voltage*1	V_{OUT}	-0.5	V_{DD} + 0.5	V
Operating Temperature	T_A	-40	85	°C
Storage temperature*2	Tstg	-40	125	°C

*1: The above parameter values are based on VSS = 0 V.

*2: The above storage temperature is the ambient temperature at which the device can be stored before the data is written, after the device is written, please refer to the working ambient temperature.

<WARNING> If the load (voltage, current, temperature, etc.) applied to the semiconductor device exceeds the maximum rated value.

Permanent destruction of the device will result, so no parameter should exceed its absolute maximum rating.

12. Recommended working conditions

parameters	notation	numerical value			unit (of measure)
		minimum value	typical value	maximum values	
Power supply voltage*1	VDD	2.7	3.3	3.6	V
Operating ambient temperature*2	TA	-40	-	+85	℃

*1: The above parameter values are based on VSS = 0V.

*2: Applies only to the ambient temperature of this chip during operation. It can be understood that this temperature is almost the same as the temperature of the chip surface.

<WARNING> To ensure proper operation of semiconductor devices, they must be used in the recommended operating environment or conditions.

All electrical characteristics are guaranteed when the device is operated under the recommended environment or conditions. Be sure to use the semiconductor device within the recommended operating environment or conditions. Exceeding this operating range may affect the reliability of the device and result in malfunction.

The Company makes no warranty as to the scope of use, operating conditions, or logic combinations not described in this data sheet. If the user wishes to use the device under conditions other than those listed, be sure to contact a sales representative in advance.

13. Electrical

DC Characteristics

(within recommended working conditions)

parameters	notation	prerequisite	numerical value			unit (of measure)
			minimum value	typical value	maximum values	
Input Leakage Current	$\|ILI\|$	V_{IN} = 0 V to V_{DD}	–	–	1	μA
Output Leakage Current	$\|ILO\|$	V_{OUT} = 0 V to V_{DD}	–	–	1	μA
Operating supply current	I_{DD}	SCK = 25MHz SO = open	–	4.2	5.5	mA
Standby Current	I_{SB}	$\overline{cs}$ = sck = si = V_{dd}	–	9	12	μA
sleep current	I_{ZZ}	$\overline{CS}$ = V_{DD} All other inputs V_{SS} or V_{DD}	–	2.8	4	μA
Input High Voltage	V_{IH}	V_{DD} = 2.7V to 3.6V	VDD * 0.7		VDD + 0.3	V
Input Low Voltage	V_{IL}	V_{DD} = 2.7V to 3.6V	-0.5		VDD * 0.3	V
Output High Voltage	V_{OH}	I_{OH} = -2 mA	VDD-0.5		VDD	V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA	VSS		0.4	V
$\overline{CS}$ pull-up resistor	R_P		18	33	80	kΩ

■ AC Characteristics

parameters	notation	numerical value		unit (of measure)
		minimum value	maximum values	
Clock frequency (commands other than FSTRD)	fCK	0	25	MHz
Clock frequency (FSTRD command)	fCK	0	40	MHz
Clock High Time	tCH	11	-	ns
Clock Low Level Time	tCL	11	-	ns
Chip Selection Setting Time	tCSU	10	-	ns
Chip Selection Hold Time	tCSH	10	-	ns
Output Disable Time	tOD	-	12	ns
Output data validity time	tODV	-	9	ns
Output Hold Time	tOH	0	-	ns
Unselect Time	tD	40	-	ns
Rise time data	tR	-	50	ns
Data drop time	tF	-	50	ns
Data setup time	tSU	5	-	ns
Data Hold Time	tH	5	-	ns
HOLD Setting time	tHS	10	-	ns
HOLD Hold time	tHH	10	-	ns
HOLD Output float time	tHZ	-	20	ns
HOLD Output activation time	tLZ	-	20	ns
SLEEP Exit Time	tREC	-	1	μs

AC test conditions

Power supply Voltage:
2.7V to 3.6V Operating
temperature range: -40°C to
+85°C

Input voltage range: $V_{DD} * 0.7 \leq V_{IH} \leq V_{DD}$, $0 \leq V_{IL} \leq V_{DD} * 0.3$
Input Rise Time :: 5 ns
Input fall time :: 5 ns
Input judgment reference level : $V_{DD} * 0.5$
Output judgment reference level : $V_{DD} * 0.5$
Output load capacitance: 30pF

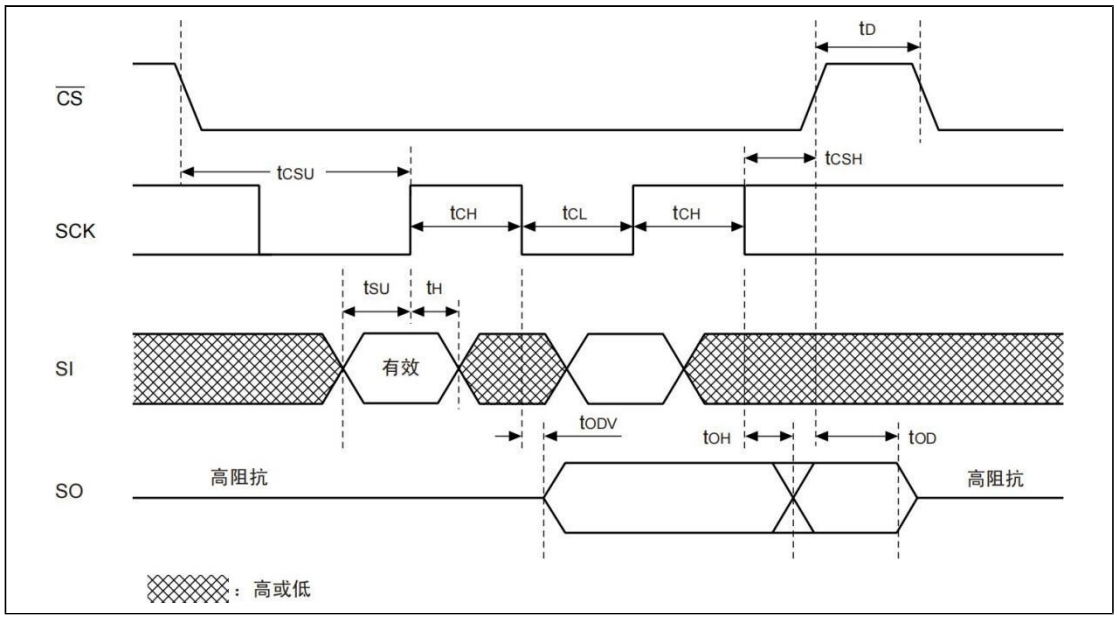
■ Pin Capacitance

parameters	notation	prerequisite	numerical value		unit (of measure)
			minimum value	maximum values	

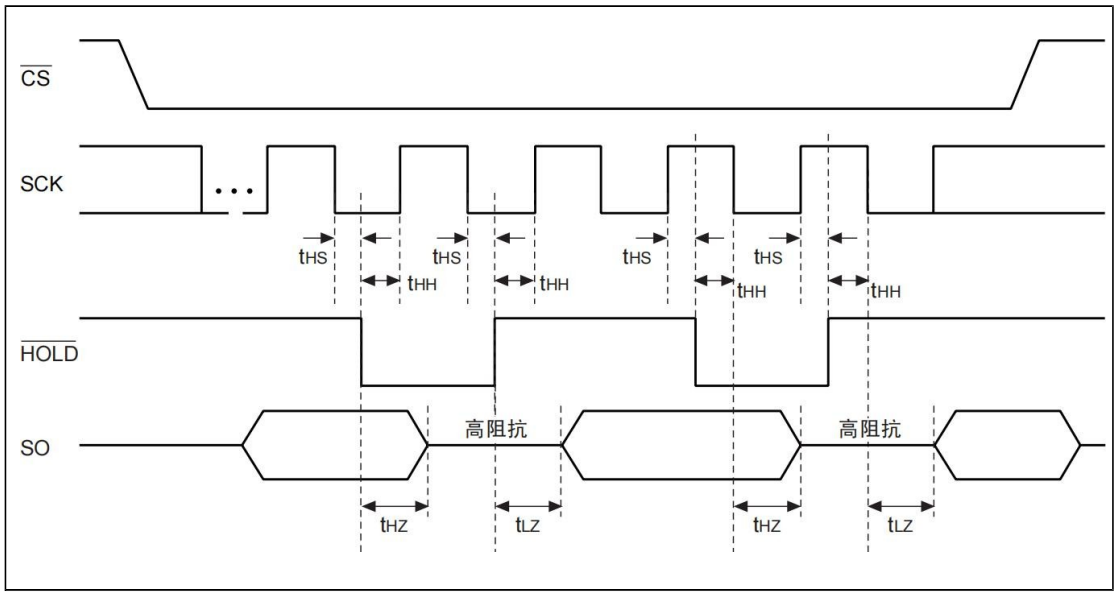
Output Capacitance	C_O	$V_{DD} = V_{IN} = V_{OUT} = 0V$. f = 1 MHz, T_A = +25°C	-	10	pF
Input Capacitance	C_I		-	10	pF

14. Timing diagrams

Serial data timing



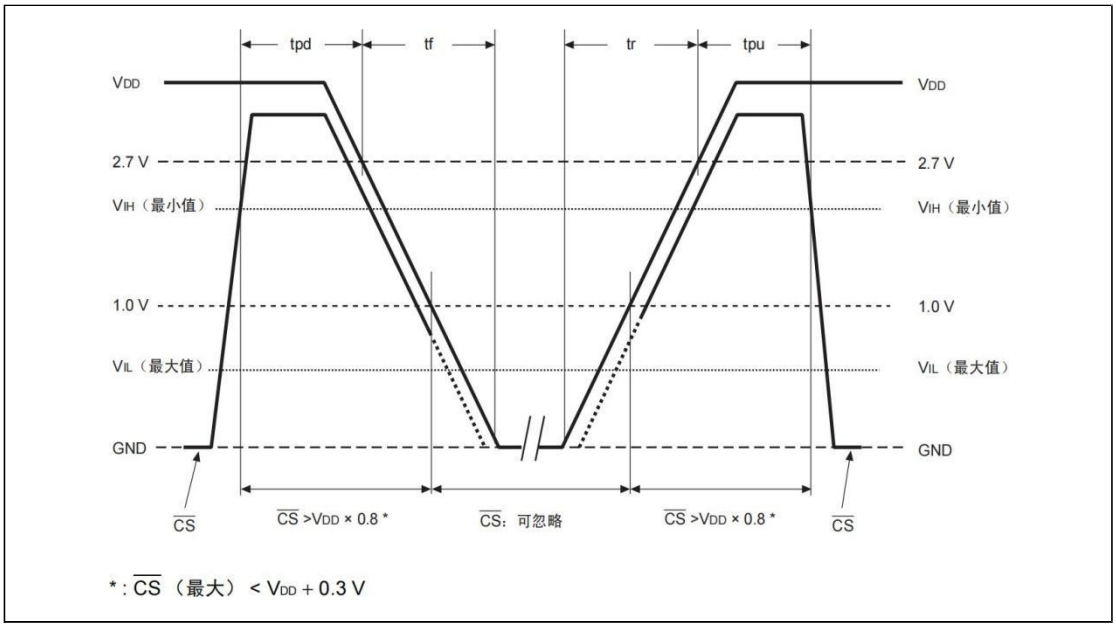
hold time (computing)



15. Power On/Off Timing

parameters	notation	numerical value		unit (of measure)
		minimum value	maximum values	
$\overline{CS}$ level hold time when power is off	tpd	200	-	ns
$\overline{CS}$ level hold time when power is turned on	tpu	5	-	μs
Power down time	tf	5	-	μs
Power Rise Time	tr	5	-	μs

Note: If the device does not operate within the specific conditions of the read cycle, write cycle, or



power-up/down timing, storage of data cannot be guaranteed.

16. FRAM characteristics

parameters	minimum value	maximum values	unit (of measure)	note
Read/write durability*1	1E6	-	times/byte	Operating ambient temperature TA = -40°C
	1E6	-	times/byte	Operating ambient temperature TA = +25°C
	1E5	-	times/byte	Operating ambient temperature TA = +85°C
Data retention*2	200	-	surname Nian	Operating ambient temperature TA = -40°C

15. Power On/Off Timing

	200	-	surname Nian	Operating ambient temperature T_A = +25°C
	10	-	surname Nian	Operating ambient temperature T_A = +85°C

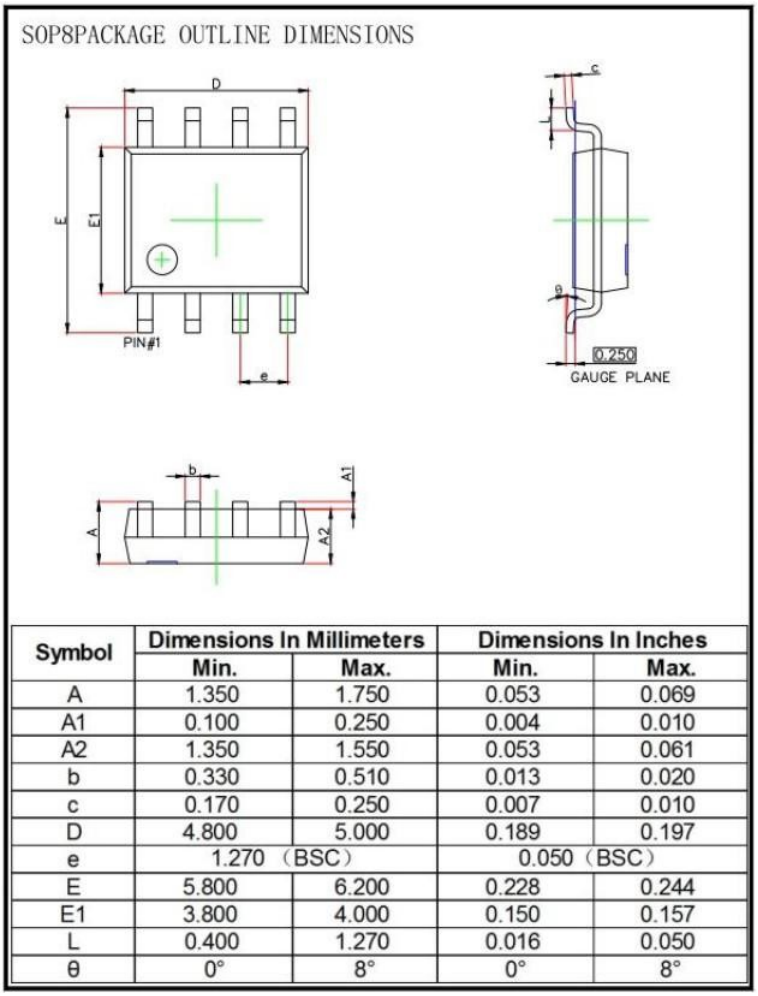
*1: Since FRAM storage operates with a destructive readout mechanism, the minimum value of read/write endurance is defined here as the sum of the number of reads and writes.

*2: The number of data retention years is the data retention time after the first read/write operation after delivery from the factory. These retention times are converted values based on the converted values derived from the results of the reliability assessment.

17. ESD and latching

test (machinery etc)	numerical value
ESD HBM (Human Body Model) Conforms to JS-001	≥2000 V|
ESD CDM (Charging Device Model) Conforms to JS-002	≥ |1000 V|
latch Conforms to JESD78	≥ |100 mA|

18. Package Size



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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