GX24C512

Ferroelectric Random Access Memory (FRAM)

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1. Description

The GX24C512 is an FRAM (Ferroelectric Random Access Memory) chip in a configuration of 65,536 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, GX24C512 is able to retain data without using a data backup battery.

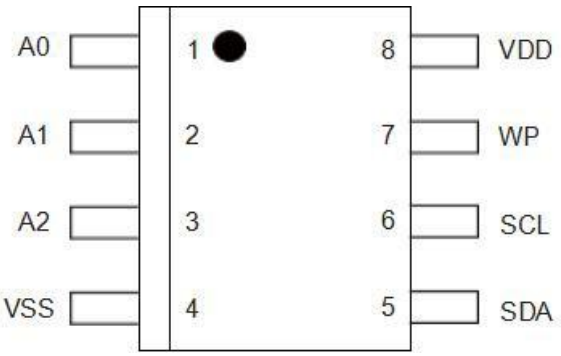
The GX24C512 does not need a polling sequence after writing to the memory such as the case of Flash memory or E2PROM.

2. Features

Capacity	65,536 words × 8bit
Interface type	I²C Interface
Operating voltage	1.7 V to 5.5 V
Operating frequency	1MHz
Operating current	0.5mA (typical @1 MHz)
Standby current	1μA (typical condition)
Endurance	6E8 times / byte (typical condition)
Data retention	10 years @ 85°C (>200 years @ 25°C)
Operation ambient temperature range	-40°C to 85°C
Package	8-pin plastic SOP RoHS compliant

3. Pin Assignment

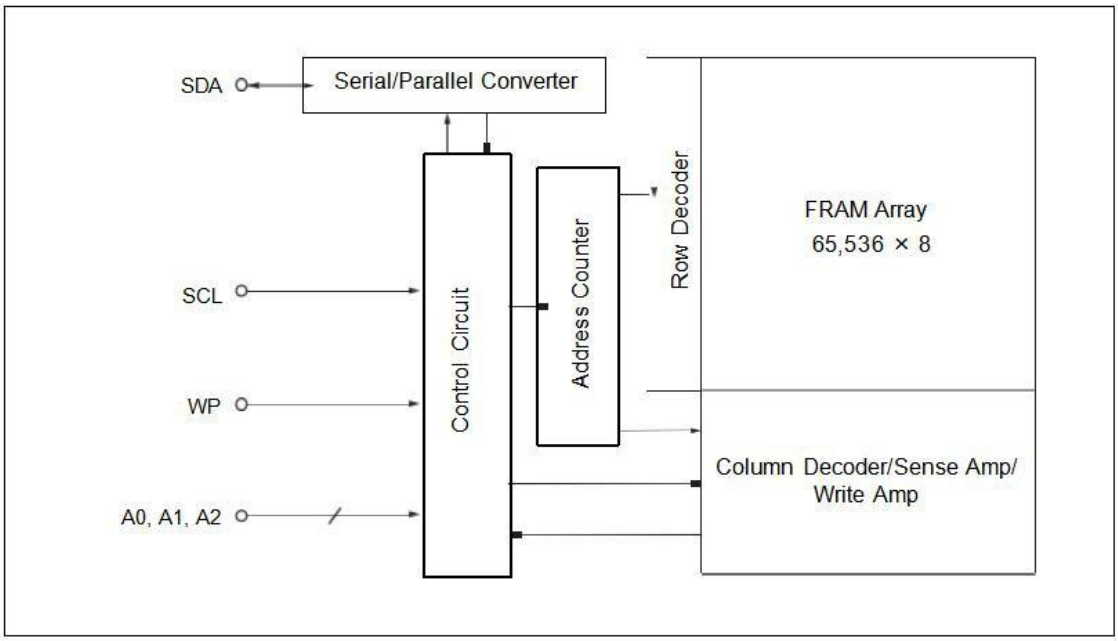
TOP VIEW



4. Pin function description

Pin Number	Pin Name	Functional Description
1 to 3	A0 to A2	Device Address pins The GX24C512 can be connected to the same data bus up to 8 devices. Device addresses are used to identify each of these devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A0, A1 and A2 pins are internally pulled-down and recognized as the "L" level.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output timing serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When the Write Protect pin is the “H” level, the writing operation is disabled. When the Write Protect pin is the “L” level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The write protect pin is internally pulled down to VSS pin, and that is recognized as the “L” level (write enabled) when the pin is the open state.
8	VDD	Supply Voltage pin

5. Block Diagram

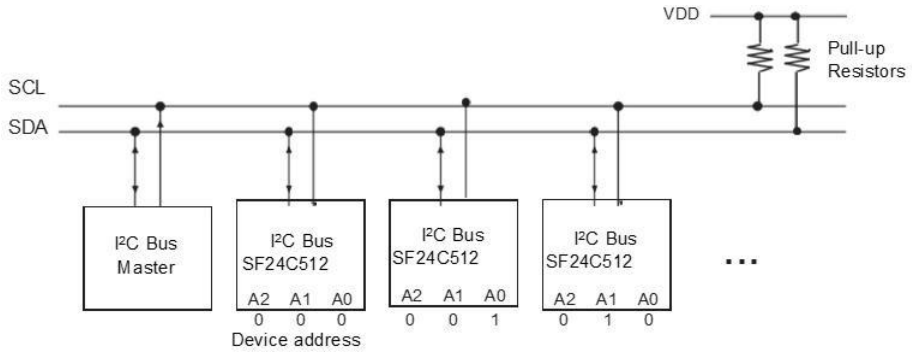


I²C (Inter-Integrated Circuit)

The GX24C512 has the two-wire serial interface; the I²C bus, and operates as a slave device.

The I²C bus defines communication roles of “ master ” and “ slave ” devices, with the master side holding the authority to initiate control. Furthermore, the I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.

I²C Interface System Configuration Example



I²C COMMUNICATION PROTOCOL

The I²C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The SDA signal should change while SCL is the "L" level. However, as an exception, when starting and stopping communication sequence, SDA is allowed to change while SCL is the "H" level.

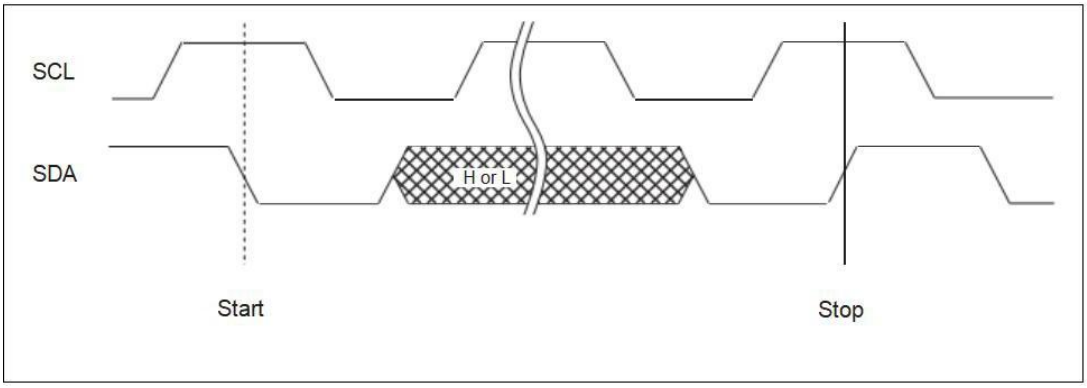
- Start Condition

To start read or write operations by the I²C bus, change the SDA input from the "H" level to the "L" level while the SCL input is in the "H" level.

- Stop Condition

To stop the I²C bus communication, change the SDA input from the "L" level to the "H" level while the SCL input is in the " H " level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

. Start Condition, Stop Condition



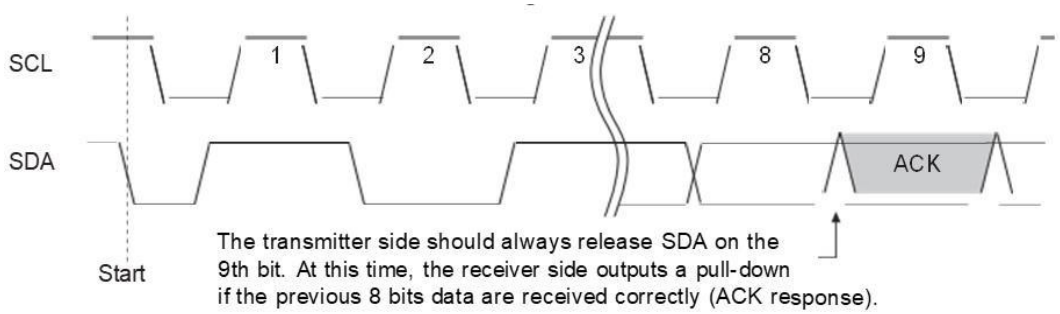
Note: At the write operation, the FRAM device does not need the programming wait time (tWC) after issuing the Stop Condition.

ACKNOWLEDGE (ACK)

In the I²C bus, serial data including address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the "L" level every time on the 9th SCL clock after each 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z released period, the receiver side pulls the SDA line down to indicate the "L" level that the previous 8 bits communication is successfully received.

In case the slave side receives Stop condition before sending or receiving the ACK "L" level, the slave side stops the operation and enters to the standby state. On the other hand, the slave side releases the bus state after sending or receiving the NACK "H" level. The master side generates Stop condition or Start condition in this released bus state.

. Acknowledge timing overview diagram



DEVICE ADDRESS WORD (Slave address)

Following the start condition, the master inputs the 8 bits device address word to start I^2C communication. The device address word (8 bits) consists of a device Type code (4 bits), device address code (3 bits) and a read/write code (1 bit).

- Device Type Code (4 bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at "1010" for the GX24C512.

- Device Address Code (3 bits)

Following the device type code, the 3 bits of the device address code are input in order of A2, A1 and A0. The device address code identifies one device from up to eight devices connected to the bus.

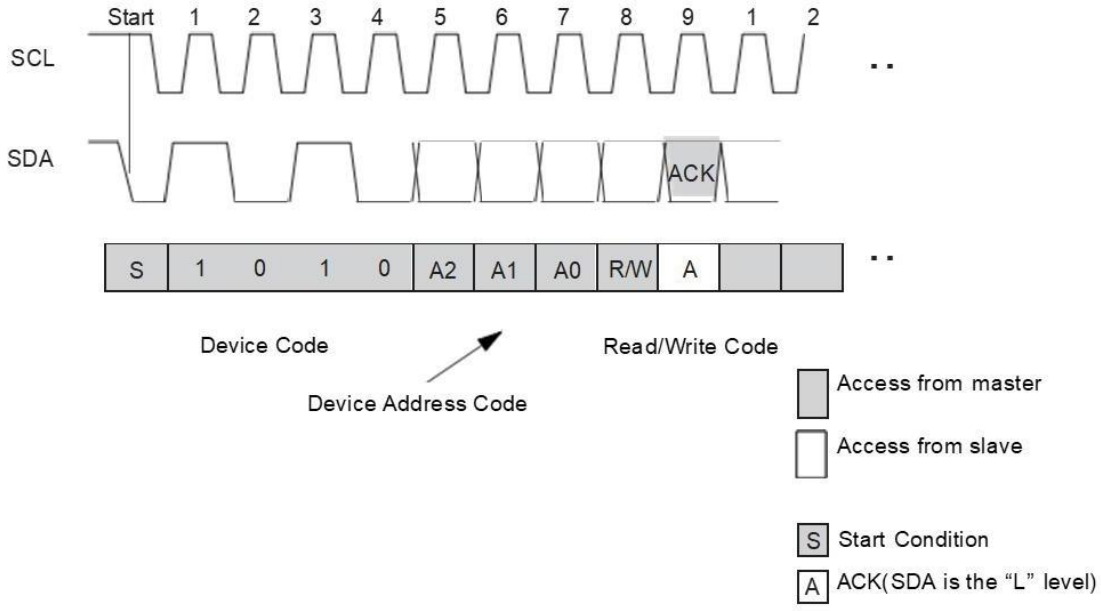
Each GX24C512 is given a unique 3 bits code on the device address pin (external hardware pin A2, A1 and A0). The slave only responds if the received device address code is equal to this unique 3 bits code.

- Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is "0", a write operation is enabled, and the R/W code is "1", a read operation is enabled for the GX24C512.

It turns to a stand-by state if the device code is not "1010" or device address code does not equal to pin A2, A1 and A0.

. **Device Address Word**



DATA STRUCTURE

In the I²C bus, the acknowledge “ L ” level is output on the 9th bit by a slave, after the 8 bits of the device address word following the start condition are input by a master. After confirming the acknowledge response by the master, the master outputs 8 bits × 2 memory address to the slave. When the each memory address input ends, the slave again outputs the acknowledge “ L ” level. After this operation, the I/O data follows in units of 8 bits, with the acknowledge “L” level output after every 8 bits.

It is determined by the R/W code whether the data line is driven by the master or the slave. However, the clock line shall be driven by the master. For a write operation, the slave will accept 8 bits from the master, then send an acknowledge. If the master detects the acknowledge, the master will transfer the next 8 bits. For a read operation, the slave will place 8 bits on the data line, then wait for an acknowledge from the master.

FRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The GX24C512 performs the high speed write operations, so any waiting time for an ACK polling* does not occur.

*: In E2PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

WRITE PROTECT (WP)

The entire memory array can be write protected using the Write Protect pin. When the Write Protect pin is set to the “H” level, the entire memory array will be write protected. When the Write Protect pin is the

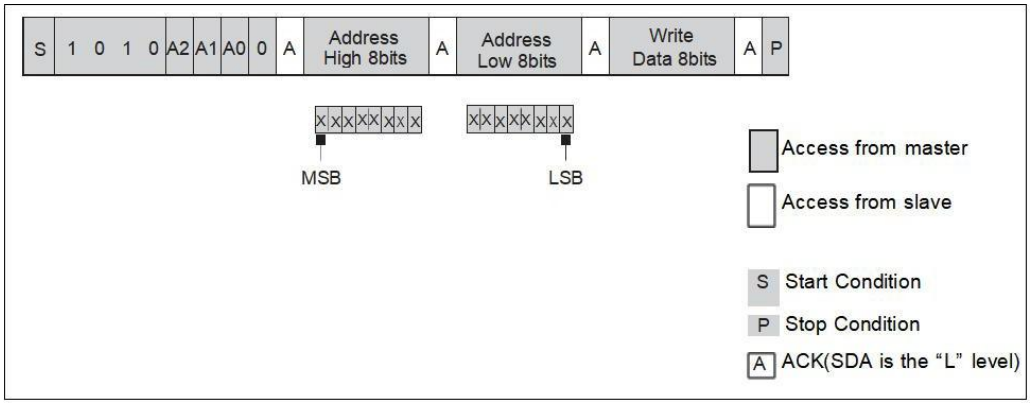
“L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

Note : The Write Protect pin is pulled down internally to the VSS pin, therefore if the Write Protect pin is open, the pin status is detected as the “L” level (write enabled).

COMMAND

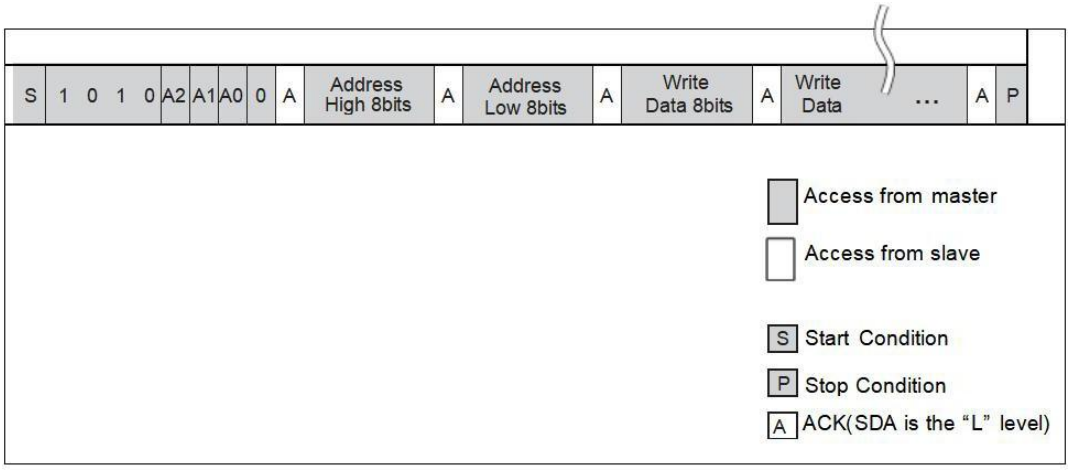
• Byte Write

If the device address word (R/W "0" input) is sent following the start condition, the slave responds with an ACK. After this ACK, write addresses and data are sent in the same way, and the write ends by generating a stop condition at the end.



• Page Write

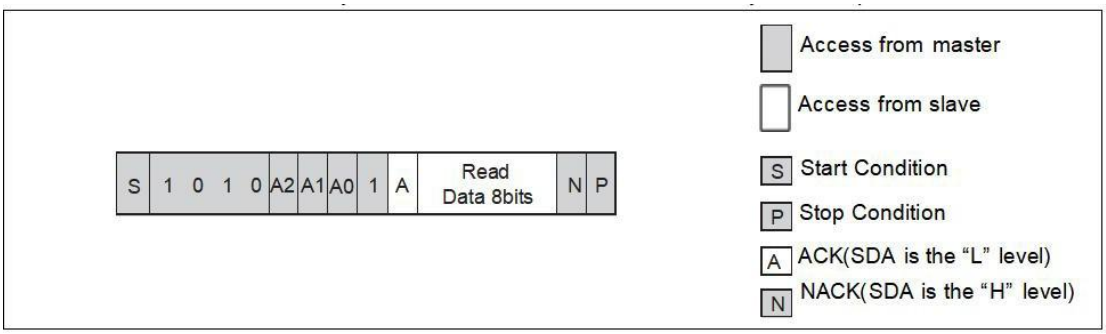
If additional 8 bits are continuously sent after the same command (except stop condition) as Byte Write, a page write is performed. The memory address rolls over to first memory address (0000H) at the end of the address. Therefore, if more than 64K bytes are sent, the data is overwritten in order starting from the start of the memory address that was written first. Because FRAM performs the high-speed write operations, the data will be written to FRAM right after the ACK response finished.



Note: It is not necessary to take a period for internal write operation cycles from the buffer to the memory after the stop condition is generated.

• Current Address Read

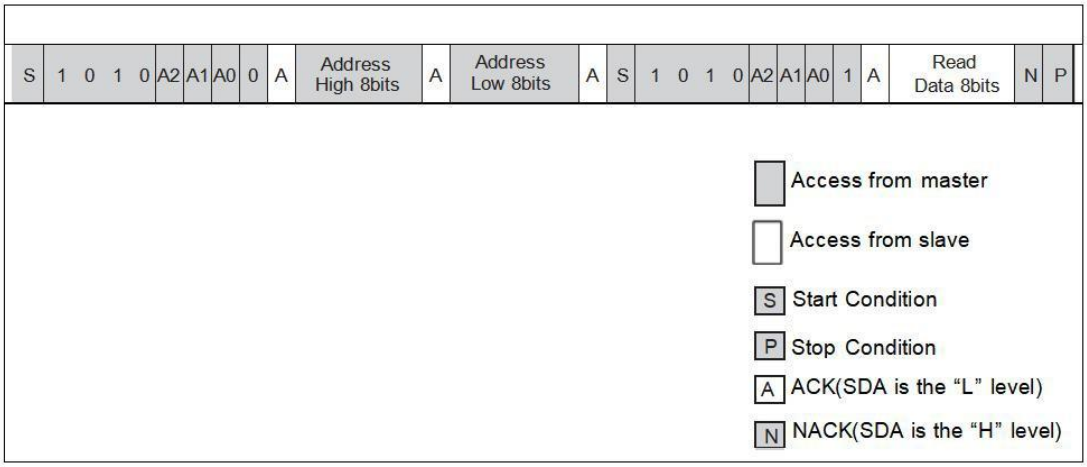
When the previous write or read operation finishes successfully up to the stop condition and assumes the last accessed address is “n”, then the address at “n+1” is read by sending the following command unless turning the power off. If the memory address is last address, the address counter will roll over to (0000H). The current address in memory address buffer is undefined immediately after the power is turned on.



• Random Read

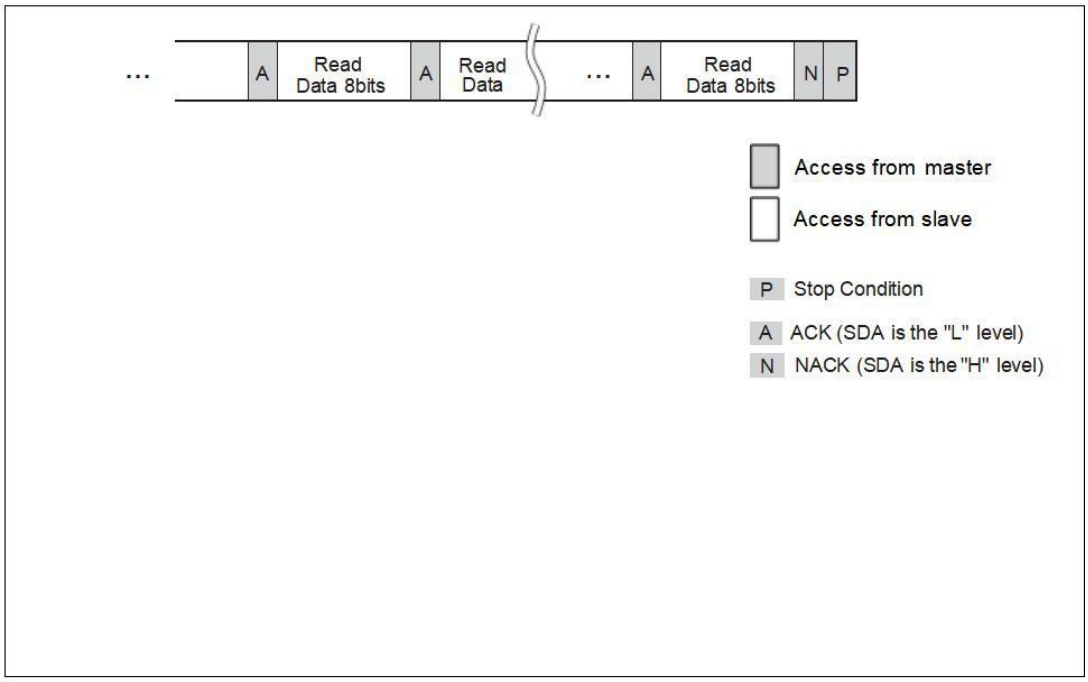
The one byte of data from the memory address saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input).

The final NACK (SDA is the “H” level) is issued by the receiver that receives the data. In this case, this bit is issued by the master
side.



• Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the internal read address automatically rolls over to first memory address (0000H) and keeps reading.



6. Absolute Maximum Rating

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	— 0.5	V_{DD} + 0.5	V
Input voltage*	V_{IN}	— 0.5	V_{DD} + 0.5	V
Output voltage*	V_{OUT}	— 0.5	V_{DD} + 0.5	V
Operation ambient temperature	T_A	— 40	+ 85	℃
Storage temperature	Tstg	— 55	+ 125	℃

* These parameters are based on the condition that VSS is 0 V.

< Warning >Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings

7. Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*	V_{DD}	1.7	—	5.5	V
"H" level input voltage*	V_{IH}	V_{DD} X 0.7	—	V_{DD}	V
" L" level input voltage*	V_{IL}	V_{SS}	—	V_{DD} X 0.3	V
Operation ambient temperature	T_A	— 40	—	+ 85	℃

* These parameters are based on the condition that VSS is 0 V.

< Warning > The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

8. Electrical Characteristics

DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	2	μA
Output leakage current*2	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}	—	—	1	μA
Operating power supply current	I_{DD}	SCL = 1 MHz	—	0.5	—	mA
Standby current	I_{SB}	SCL, SDA = V_{DD} A0, A1, A2, WP = 0 V or V_{DD} or Open Under Stop Condition T_A = + 25 °C	—	1	—	μA
"L" level output voltage	V_{OL}	I_{OL} = 3 mA	—	—	0.4	V
Input resistance for WP, A0, A1 and A2 pins	R_{IN}	V_{IN} = V_{IL} (Max)	50	—	—	kΩ
		V_{IN} = V_{IH} (Min)	1	—	—	MΩ

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

AC Characteristics

Parameter	symbol	Value		unit
		Min	Max	
SCL clock frequency	FSCL	0	1000	kHz
Clock high time	T_{HIGH}	260	—	ns
Clock low time	T_{LOW}	500	—	ns
SCL/SDA rising time	T_r	—	300	ns
SCL/SDA falling time	T_f	—	100	ns
Start condition hold	$T_{HD:STA}$	250	—	ns
Start condition setup	$T_{SU:STA}$	250	—	ns
SDA input hold	$T_{HD:DAT}$	0	—	ns
SDA input setup	$T_{SU:DAT}$	50	—	ns
SDA output hold	$T_{DH:DAT}$	0	—	ns
Stop condition setup	$T_{SU:STO}$	250	—	ns
SDA output access after SCL falling	T_{AA}	—	450	ns
Pre-charge time	T_{BUF}	500	—	ns
Noise suppression time (SCL and SDA)	T_{SP}	—	50	ns

AC characteristics were measured under the following measurement conditions.

Power supply voltage : 1.7 V to 5.5 V

Operation ambient temperature : -40° C to + 85° C

Input voltage magnitude : V_{DD} X 0.2 to V_{DD} X 0.8

Input rising time : 5 ns

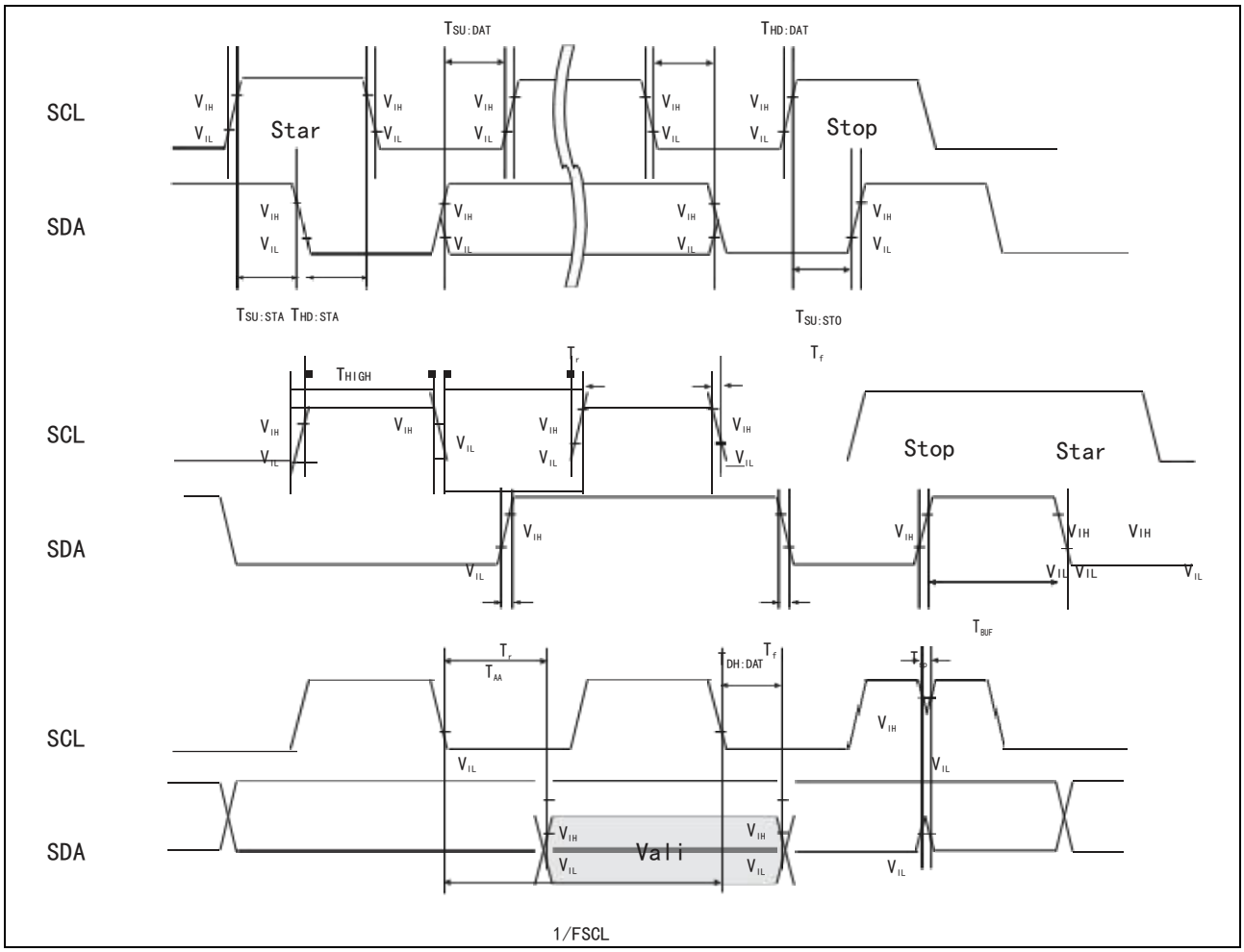
Input falling time : 5 ns

Input judge level : $V_{DD}/2$

Output judge level : $V_{DD}/2$

Output load capacitance : 100 pF

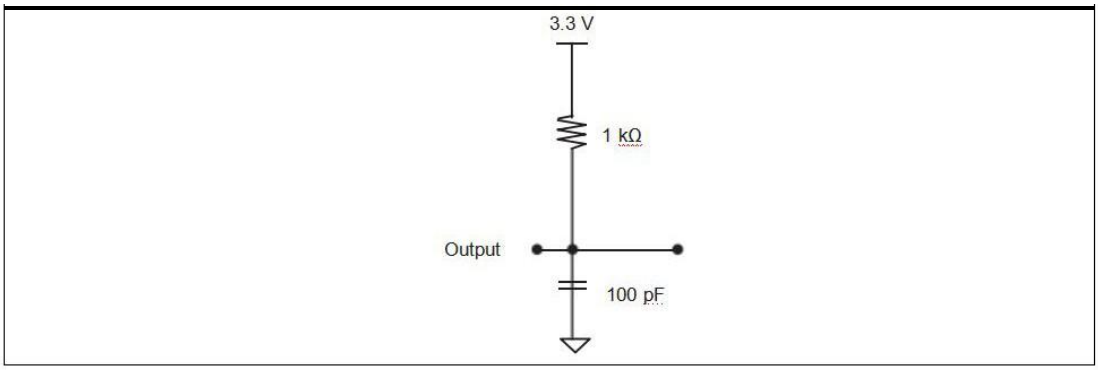
9. Timing Diagram



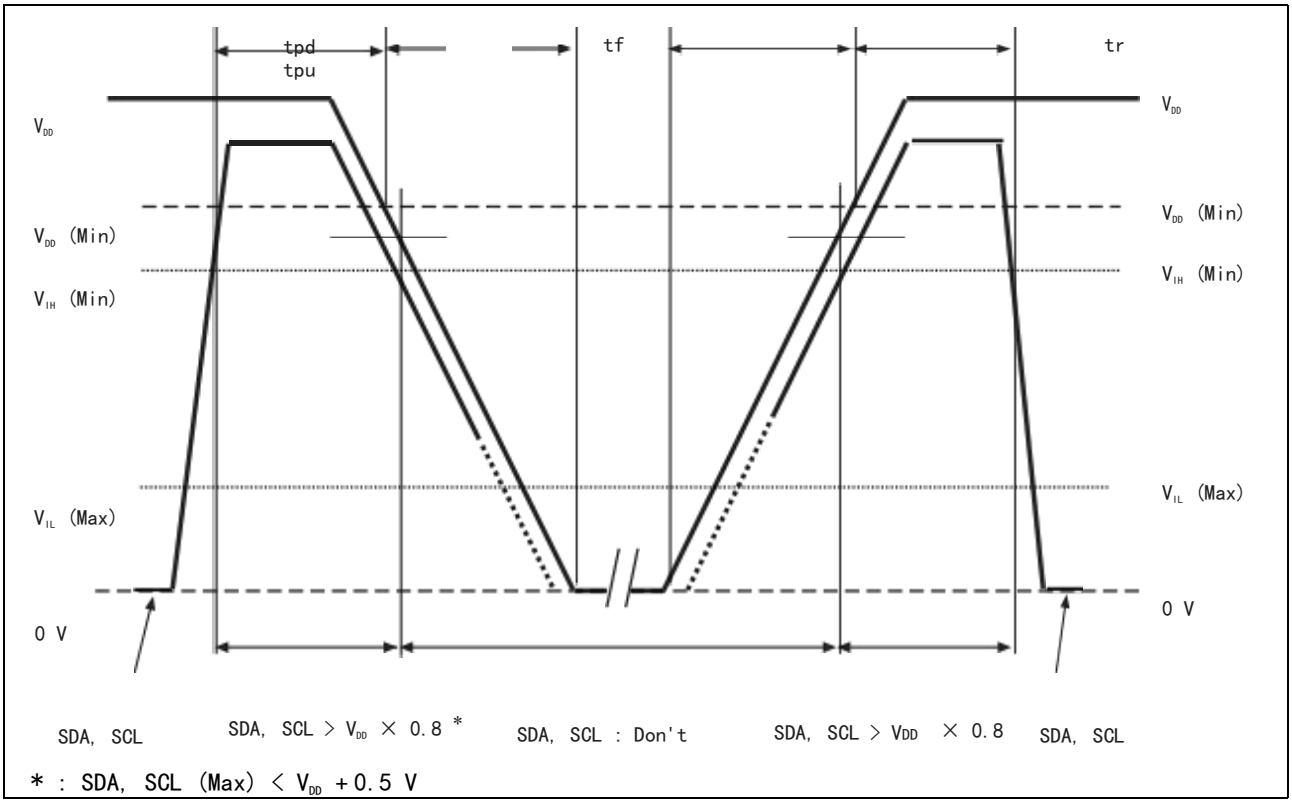
Pin capacitance

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
I/O capacitance	$C_{I/O}$	V_{DD} = 3.3 V, f = 1 MHz, T_A = + 25 °C	—	8	pF
Input capacitance	C_{IN}		—	8	pF

AC Test Load Circuit



10. Power On/off Sequence



Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85	—	ns
SDA, SCL level hold time during power up	tpu	250	—	µs
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V
Internal regulator recovery time	t_{REC}	—	400	µs

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

11. FRAM Characteristics

Parameter	Min	Max	Unit	Remark
Read/Write Endurance*1	6E8	—	Times/byte	Operation Ambient Temperature T_A = + 25 °C
Data Retention* 2	10	—	Years	Operation Ambient Temperature T_A = + 8 5 °C

*1: Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

12. NOTE ON USE

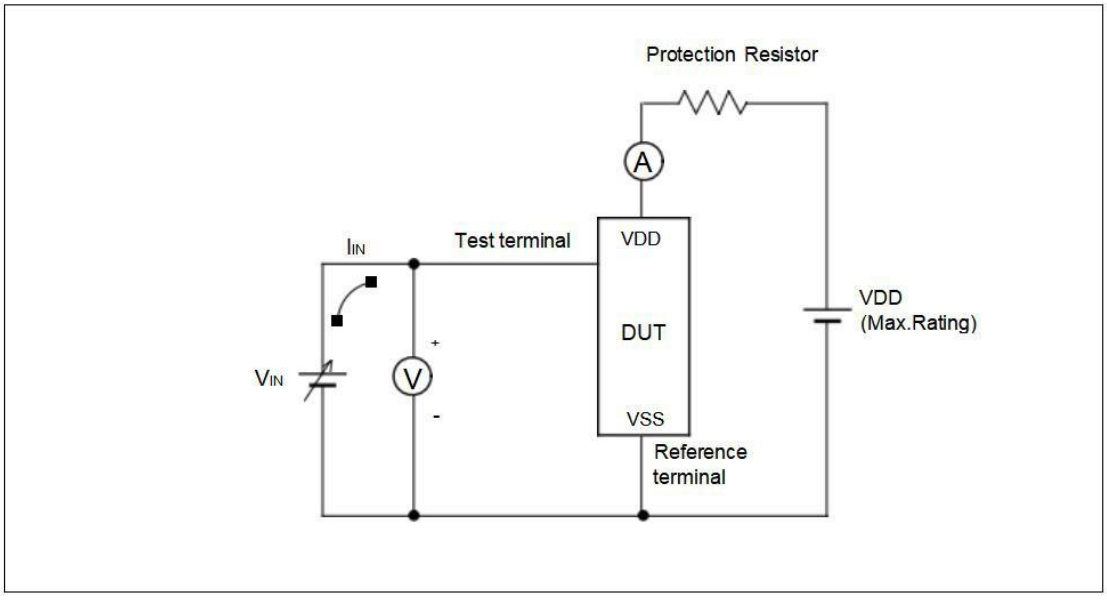
• We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

• During the access period from the start condition to the stop condition, keep the level of WP, A0, A1 and A2 pins to the “H” level or the “L” level.

13. ESD and Latch-Up

Test	DUT	Numerical value
ESD HBM (Human Body Model) JESD22-A114 compliant	GX24C512	≥| 2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥| 200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		—
Latch-Up (I-test) JESD7 8 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD7 8 compliant		—
Latch-Up (Current Method) Proprietary method		—
Latch-Up (C-V Method) Proprietary method		—

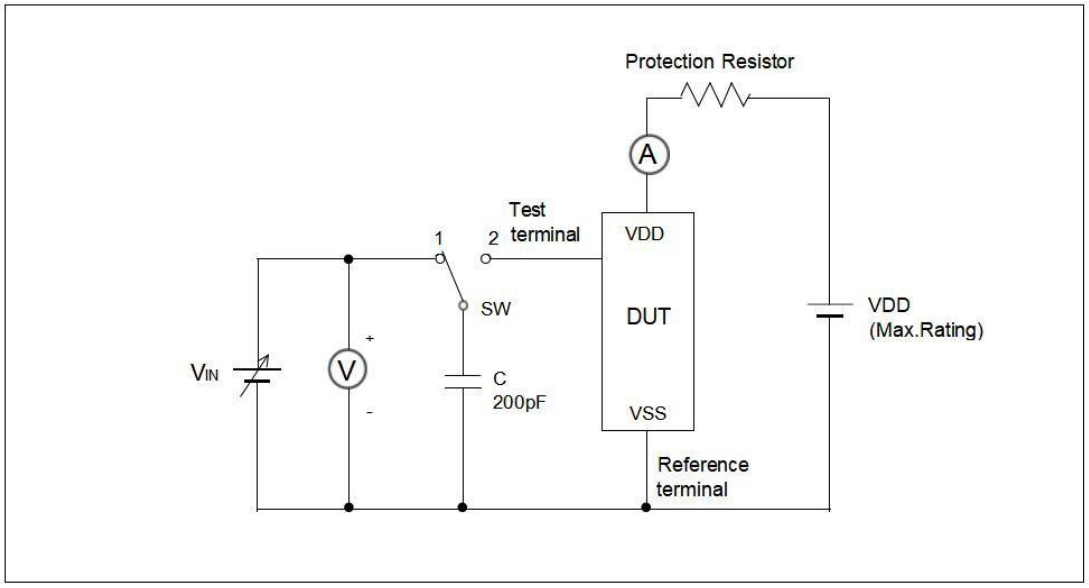
- Current method of Latch-Up Resistance Test



Note: The voltage VIN is increased gradually and the current IIN of 300 mA at maximum shall flow. Confirm the latch up does not occur under IIN = ±300 mA.

In case the specific requirement is specified for I/O and IIN cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

• C-V method of Latch-Up Resistance Test



Note: Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.

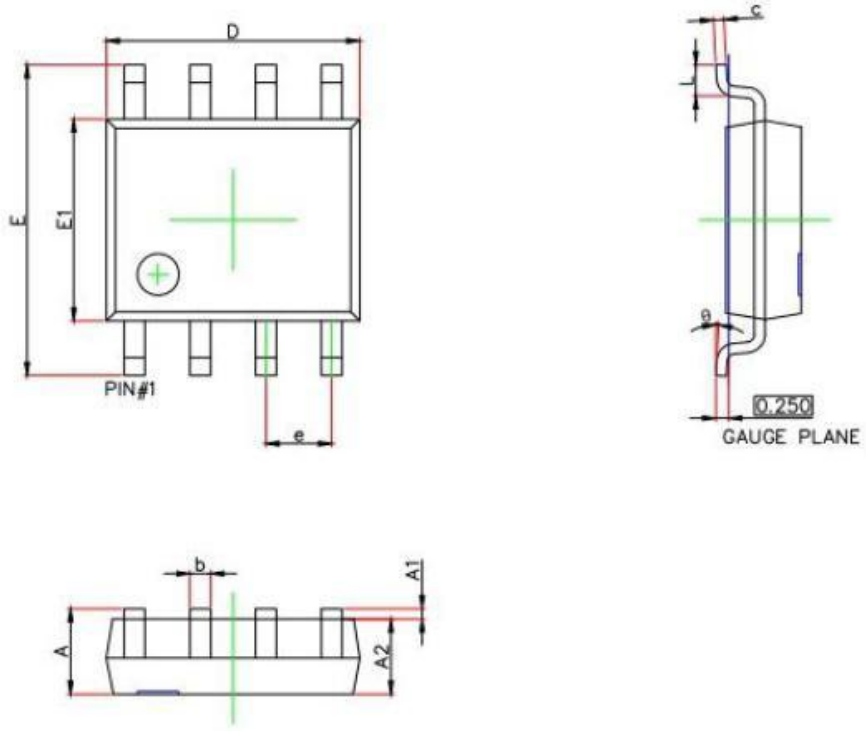
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

• REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL]: Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

14. Package Dimension

SOP8PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 （BSC）		0.050 （BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

15. Ordering Information

Example: S F 24C 512 __ - W S H - I R

Company prefix
S=Smart Memories

Product family
F=FRAM

Interface
24C=I²C Interface

Device density
512=512Kb

Version
Blank=A Version
B=B Version
C=C Version

Operating voltage
N=2.7~3.6V
W=1.7~5.5V
V=1.8~5.5V

Package
S=SOP8 150mil
T=TSSOP8
U=UDFN2*3

Green Standard
H=RoHS Compliant

Device Grade
C=Consumer Grade, T= -25℃ to 60℃
I=Industrial Grade, T= -40℃ to 85℃

Packing type
T=Tube
R=Tape&Reel
Y=Tray

16. Revision History

Revision	Date	Description
V1.0	2024/3/1	Initial version

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