# GX9208 14 Bit，3GSPS， JESD204B ， Dual ADC

## FEATURES

- JESD204B (Subclass 1) coded serial digital outputs Support for lane rates up to 15 Gbps per lane
- 1.5 W total power per channel at 3 GSPS (default settings)
- DC supply：0.975 V、1.9V 和 2.5 V
- Amplitude detect bits for efficient AGC implementation
- Serial port control
  Integer clock with divide by 2 and divide by 4 options
  Flexible JESD204B lane configurations
- On-chip dither
- 2 integrated, wideband digital processors per channel
  48 -bit NCO
  4 cascaded half-band filters

## APPLICATIONS

- Diversity multiband and multimode digital receivers
- 3G/4G、TD-SCDMA、W-CDMA、GSM、LTE、LTE-A
- Electronic test and measurement systems
- Phased array radar and electronic warfare
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

## FUNCTIONAL BLOCK DIAGRAM

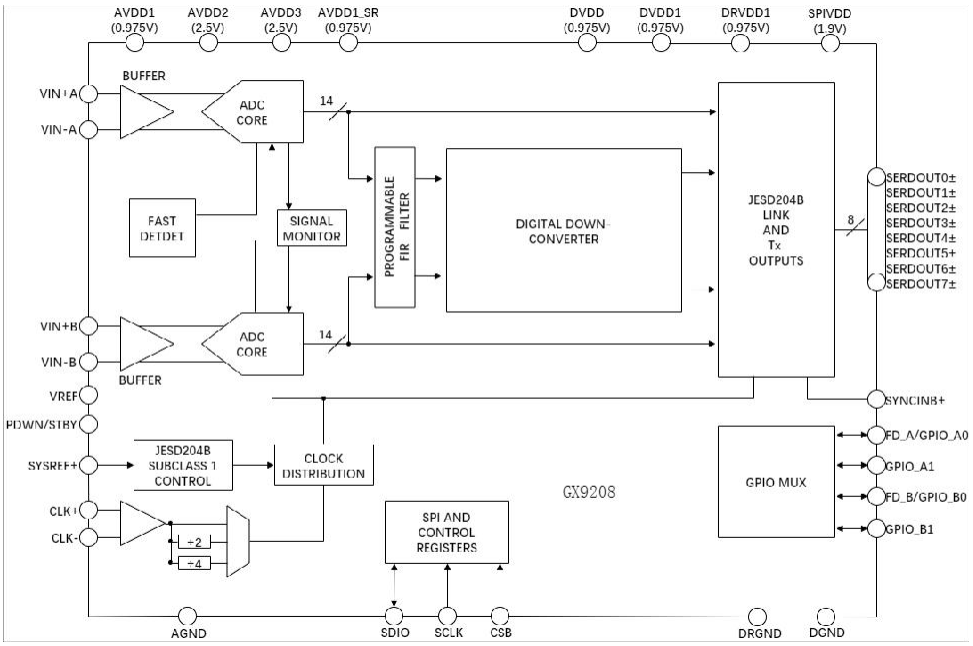


Figure 1 Functional Module Diagram

## CONTENTS

## GENERAL DESCRIPTION

The GX9208 is a dual, 14-bit, 3 GSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of direct sampling wide bandwidth analog signals of up to 5 GHz. The GX9208 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The analog input and clock signals are differential inputs.

The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x0245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the GX9208 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

The user can configure the Subclasss 1 JESD204B-based high speed serialized output in a variety of one-lane, two-lane, four-lane, and eight-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The GX9208 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 3-wire serial port interface (SPI).

The GX9208 is available in a 196-ball BGA, specified over the −40°C to +85°C ambient temperature range.

## PRODUCT HIGHLIGHTS

- Supports direct radio frequency (RF) sampling of signals up to about 5 GHz.
- A SPI controls various product features and functions to meet specific system requirements.
- Programmable fast overrange detection and signal monitoring.
- 12 mm × 12 mm, 196-ball BGA, On-chip temperature diode for system thermal management.

## SPECIFICATIONS

### DC SPECIFICATIONS

AVDD1 = 0.975V，AVDD1 _SR= 0.975V, AVDD3 = 2.5V, DVDD = 0.975V, DRVDD1 = 0.975V, SPIVDD = 1.9V, specified maximum sampling rate，1.6 $V_{P-P}$full-scale differential input, input amplitude $A_{IN}$ = −2.0 dBFS，L=8，M=2，F=1，−10°C≤$T_J$≤+120°C[1]. unless otherwise noted. Typical specifications represent performance at $T_J$=70°C（$T_A$=25°C）.

Table 1 ADC DC Specifications

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Resolution | | 14 | | Bit |
| No Missing Codes | | Guaranteed | | |
| Offset Error | | 0 | | %FSR |
| Gain Error | | | | %FSR |
| Gain Matching | | 0.7 | | %FSR |
| Differential Nonlinearity（DNL） | | ±0.66 | | LSB |
| Integral Nonlinearity ( INL） | | ±6 | | LSB |
| Internal Voltage Reference | | 1 | | V |
| Input-referred noise | | 5 | | LSB rms |
| Analog Differential Input Voltage Range | 1.1 | 1.6 | 1.6 | $V_{P-P}$ |
| Differential Input Capacitance | | 0.35 | | pF |
| Common-Mode Voltage（$V_{CM}$） | | 1.4 | | V |
| AVDD1 Supply Voltage | 0.95 | 0.975 | 1.0 | V |
| AVDD3 Supply Voltage | 2.44 | 2.5 | 2.56 | V |
| DVDD Supply Voltage | 0.95 | 0.975 | 1.0 | V |
| DRVDD1 Supply Voltage | 0.95 | 0.975 | 1.0 | V |
| SPIVDD Supply Voltage | 1.85 | 1.9 | 1.95 | V |
| $I_{AVDD1}$ Supply Current | | 95 | | mA |
| $I_{AVDD3}$ Supply Current | | 840 | | mA |
| $I_{DVDD}$ Supply Current | | 800 | | mA |
| $I_{DRVDD1}$ Supply Current [2] | | 50 | | mA |
| $I_{SPIVDD}$ Supply Current | | 0.5 | | mA |
| Total Power Dissipation | | 2.998 | | W |
| Power-Down Dissipation | | 93.3 | | mW |

(1) The junction temperature ($T_J$) range of −10°C to +120°C translates to an ambient temperature ($T_A$) range of −40°C to +85°C.
(2) All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.
(3) Can be controlled by the SPI.